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1 – Device Architecture

FPGA Architecture

This section presents an overview of the SmartFusion™ FPGA fabric, which provides a general description of the FPGA architecture and routing resources.

VersaTile

Based upon successful Actel ProASIC® 3 logic architecture, Actel SmartFusion devices provide granularity comparable to gate arrays. The SmartFusion device FPGA fabric consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 1-1, a logic VersaTile cell has four inputs and one output. Each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input combinatorial function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the combinatorial and sequential cells of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet or global network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 1-1).

Note: *This input can only be connected to the global clock distribution network.

Figure 1-1 • SmartFusion Core VersaTile
Array Coordinates

During many place-and-route operations performed by the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 1-1 is provided as a reference. The array coordinates are measured from the lower left (0, 0) corner. They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

Table 1-1 provides array coordinates of core cells and memory blocks.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and edge core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 1-1. The Designer ChipPlanner tool provides array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 1-2 illustrates the array coordinates of an A2F200 device. For more information on how to use array coordinates for region/placement constraints, see the Designer User's Guide or online help (available in the software) for SmartFusion software tools.

### Table 1-1 • Array Coordinates

<table>
<thead>
<tr>
<th>Device</th>
<th>VersaTiles</th>
<th>Memory Rows</th>
<th>All</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Minimum x (x, y)</td>
<td>Minimum y (y, y)</td>
<td></td>
</tr>
<tr>
<td>A2F200</td>
<td>3</td>
<td>2</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>37</td>
<td>37</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(0, 0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(133, 41)</td>
</tr>
</tbody>
</table>

Note: The vertical I/O tile coordinates are not shown. West side coordinates are ((0, 2) to (2, 2)) to ((0, 41) to (2, 41)); east side coordinates are ((131, 2) to (133, 2)) to ((131, 39) to (133, 39)).

Figure 1-2 • Example of Using FPGA Fabric Array Coordinates for A2F200 (does not show device feature locations)
Routing Architecture

The routing structure of SmartFusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet global networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 1-3). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire SmartFusion FPGA fabric (Figure 1-4 on page 8). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: a length of +/–12 VersaTiles in the vertical direction and a length of +/–16 VersaTiles in the horizontal direction from a given core VersaTile (Figure 1-5 on page 9). Very long lines in SmartFusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 1-6 on page 11). These routes are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew or least penalty of fanout on net delays. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.

![Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors](image)

Note: Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.

*Figure 1-3 • Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors*
Figure 1-4 • Efficient Long-Line Resources

- Spans Four VersaTiles
- Spans Two VersaTiles
- Spans One VersaTile

VersaTile

- Spans One VersaTile
- Spans Two VersaTiles
- Spans Four VersaTiles
Figure 1-5 • Very-Long-Line Resources
Global Resources (VersaNets)

SmartFusion devices offer powerful and flexible control of circuit timing through the use of clock conditioning circuitry (CCC). The SmartFusion FPGA fabric has six CCCs, which include access to at least one PLL core that is controlled by the microcontroller subsystem (MSS). The shared PLL is part of the microcontroller clock circuitry (MCC) and is configured by firmware running on the microcontroller. Users have the option of using Actel’s Libero® Integrated Design Environment (IDE) MSS Configuration Graphical User Interface to define the MCC configuration or can use the Actel System Boot Firmware to achieve the same result. Alternatively, users can create custom firmware to setup the MCC Configuration Registers. For more information, refer to the appropriate clock circuitry description in the “PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators” section of the SmartFusion Microcontroller Subsystem User’s Guide. The PLL includes a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six lines total). The CCCs at the four corners each have access to three quadrant global lines on each quadrant of the chip.

Advantages of the VersaNet Approach

One of the architectural benefits of SmartFusion is the set of powerful and low-delay VersaNet global networks. SmartFusion offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 1-6 on page 11). In addition, SmartFusion devices have three regional globals (quadrant globals) in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks. There are a total of 18 global networks on the device. Each of these networks contains spines and ribs that reach all VersaTiles in all quadrants (Figure 1-7 on page 12). This flexible VersaNet global network architecture allows users to create a total number of clock networks equal to the total number of global spines in the device. Details on the VersaNet networks are given in Table 1-2 on page 12. The flexibility of the SmartFusion VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping timing-critical, high-fanout nets to the VersaNet global network.
Figure 1-6 • Overview of SmartFusion VersaNet Global Network
Figure 1-7 • Global Network Architecture

Table 1-2 • Globals/Spines/Rows by Device

<table>
<thead>
<tr>
<th></th>
<th>A2F200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global VersaNets (trees)* / Quadrant</td>
<td>9</td>
</tr>
<tr>
<td>VersaNet Spines/Tree</td>
<td>8</td>
</tr>
<tr>
<td>Total Spines</td>
<td>72</td>
</tr>
<tr>
<td>VersaTiles in Each Top Spine</td>
<td>384</td>
</tr>
<tr>
<td>VersaTiles in Each Bottom Spine</td>
<td>768</td>
</tr>
<tr>
<td>Total VersaTiles = 4 × (384 + 768)</td>
<td>4,608</td>
</tr>
</tbody>
</table>

Note: *There are six chip (main) globals and three globals per quadrant.
VersaNet Global Networks and Spine Access

The SmartFusion architecture contains a total of 18 segmentable global networks that can access the VersaTiles, SRAM, and I/O tiles on the SmartFusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using each available device spine for internal/external clocks or other high-fanout nets in SmartFusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on SmartFusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 1-7 on page 12).

The spines are the vertical branches of the global network tree, shown in Figure 1-6 on page 11. Each spine in a vertical column of a chip (main) global network is further divided into two spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the SmartFusion device (the "scope" of the spine; see Figure 1-6 on page 11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 1-8). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 1-8. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device.

Figure 1-8 • Spine-Selection MUX of Global Tree

SmartFusion A2F200 VersaNet Topology

Figure 1-9 is an example of a global tree used for clock routing. The global tree presented in Figure 1-9 is driven by a CCC located on the west side of the device. It is used to drive all D-flip-flops.
in the device. For device-specific VersaNet timing characteristics, refer to the "DC and Switching Characteristics" chapter of the *SmartFusion Intelligent Mixed-Signal FPGAs* datasheet.

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to build domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 1-10 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib.

---

**Figure 1-9** • Example of Global Tree Used in an A2F200 Device for Clock Routing

**Figure 1-10** • Clock Aggregation Tree Architecture
This section describes the clocking resources available to the SmartFusion™ FPGA fabric. Some of the resources are embedded within the SmartFusion microcontroller subsystem (MSS), but provide the FPGA fabric with access to internal and external clock signals.

The SmartFusion device family has a robust collection of clocking peripherals, some of which are shared between the SmartFusion FPGA fabric and the microcontroller subsystem.

Figure 2-1 provides a top-level representation of the clocking resources available to the SmartFusion FPGA fabric. As shown in Figure 2-1, there is an MSS clock conditioning circuit (CCC) that contains a PLL. This MSS CCC is primarily configured via firmware running on the ARM® Cortex™-M3 processor and is shared between the MSS and FPGA fabric. Users have the option of using Actel's Libero® Integrated Design Environment (IDE) MSS configurator to configure the MSS CCC and Actel System Boot Firmware. Alternatively, users can create custom firmware to setup the MSS CCC Configuration Registers. For more information about configuring the MSS clocking resources, refer to the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" section of the SmartFusion Microcontroller Subsystem User's Guide. Additionally, there are five standard CCCs dedicated to the FPGA fabric. In the A2F200 device, the standard CCCs do not integrate a PLL.

![Figure 2-1 • SmartFusion Device Clocking Resources](image-url)
Table 2-1 provides a list view representation of the various clocking sources that can drive a clock signal into the SmartFusion FPGA fabric grouped by the device resources used to route the input clock to the FPGA fabric.

Table 2-1 • SmartFusion FPGA Clocking Sources

<table>
<thead>
<tr>
<th>Input Clock Source</th>
<th>Clocking Resource Used to Route Clock to Fabric</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 MHz RC oscillator</td>
<td>MSS_CCC</td>
<td>This is an internal RC oscillator.</td>
</tr>
<tr>
<td>32 KHz low-power crystal oscillator</td>
<td>MSS_CCC</td>
<td>Requires external crystal.</td>
</tr>
<tr>
<td>32 KHz – 20 MHz oscillator</td>
<td>MSS_CCC</td>
<td>Requires external crystal or RC circuit</td>
</tr>
<tr>
<td>Derived clock routed from FPGA fabric</td>
<td>MSS_CCC</td>
<td>During Cortex-M3 boot at power-up, CLKC source is set to internal RC oscillator (100 MHz) and divided by 4 such that both GLA and GLC outputs are fixed at 25 MHz. GLB bypasses PLL and outputs clock sourced from global I/O buffer. After power-up, user firmware can reconfigure the CLKA, CLKB or CLKC sources to be sourced from the FPGA fabric. Refer to the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the <em>SmartFusion Microcontroller Subsystem User’s Guide</em>.</td>
</tr>
<tr>
<td>FPGA Fabric CCC</td>
<td>Actel primitive macros such as CLKDLKY or CLKINT should be instantiated in user design.</td>
<td></td>
</tr>
<tr>
<td>External clock from global I/O pad</td>
<td>GLA1 of MSS_CCC</td>
<td>During Cortex-M3 boot at power-up, GLA1 output fixed at 25 MHz until user-defined configuration is applied. Refer to the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the <em>SmartFusion Microcontroller Subsystem User’s Guide</em>.</td>
</tr>
<tr>
<td>GLB of MSS_CCC</td>
<td>GLB can be used to output an FPGA fabric ONLY clock signal not tied to MSS clock frequency if configured to bypass the PLL and source the input clock from a CLKB global I/O Buffer. Refer to the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the <em>SmartFusion Microcontroller Subsystem User’s Guide</em>.</td>
<td></td>
</tr>
<tr>
<td>GLC of MSS_CCC</td>
<td>1) At power-up, during Cortex-M3 boot, CLKC is set to internal RC oscillator (100 MHz) and divided by 4 such that GLC output fixed at 25 MHz until user defined configuration is applied through firmware.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2) GLC optionally shared with FPGA fabric and MSS Ethernet MAC.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Refer to the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the <em>SmartFusion Microcontroller Subsystem User’s Guide</em>.</td>
<td></td>
</tr>
<tr>
<td>FPGA Fabric CCC</td>
<td>Configured by Programming FPGA fabric</td>
<td></td>
</tr>
</tbody>
</table>

Note: *The microcontroller clock conditioning circuitry (MSS_CCC) can be configured using Libero IDE’s MSS configurator software tool or by user firmware running on the Cortex-M3 processor. Refer to the Libero IDE Online Help and the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User’s Guide* for more information.*
Dedicated FPGA Clock Conditioning Circuits without PLL

In the SmartFusion A2F200 device, there are five CCCs dedicated to the FPGA fabric, as shown in Figure 2-1 on page 15. The CCCs located in the corners of the device allow access to the quadrant global routing within the SmartFusion FPGA fabric, while the CCCs located at the middle of the device drive chip-level global lines.

Each of the FPGA CCCs without PLL can implement up to three independent global buffers (with or without programmable delay). A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC. The FPGA CCC block is configurable via flash configuration bits set in the programming bitstream.

Each global buffer can be driven from one of the following:
- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- An internal net from the FPGA fabric

Figure 2-2 provides a simplified block diagram of the physical implementation of the building blocks in each of the SmartFusion FPGA CCCs.

![Figure 2-2 • Overview of the FPGA CCCs Offered in SmartFusion](image-url)
Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-3).

The CLKINT macro provides a global buffer function driven by the FPGA fabric.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by SmartFusion devices.

![Figure 2-3 • Global Buffers with No Programmable Delay](image-url)
Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-4). The CLKDLY macro takes the selected clock input and adds a user-defined delay. This macro generates an output clock phase shift from the input clock.

- The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations. Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the SmartFusion family.
- The CLKDLY macro can be driven directly from the FPGA fabric.
- The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier in the “Dedicated FPGA Clock Conditioning Circuits without PLL” section on page 17.

The visual CLKDLY configurator in the SmartGen tool of the Libero® Integrated Design Environment (IDE) and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

---

**Figure 2-4**  •  SmartFusion CCC Options: Global Buffers with Programmable Delay
Global Input Selections

Each global buffer, as well as the PLL reference clock, can be driven from one of the following (Figure 2-5):

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA fabric

Notes:
1. Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric.
2. Instantiate the routed clock source input as follows:
   a) Connect the output of a logic element to the clock input of the PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVDS/LVPECL) in a relevant global pin location.

Sample Pin Names

GAA0, GAA1, GAA2: GA represents global in the northwest corner of the device. A[0:2]: designates specific A clock source.

Source for CCC (CLKA or CLKB or CLKC)

Routed Clock (from FPGA core)

Figure 2-5 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT

If the single-ended I/O standard is selected, there is flexibility to choose one of the global input pads (the first, second, and fourth input). The other two global I/O locations are used as regular I/Os. If the differential I/O standard is chosen, the first and second inputs are considered to be paired, and the third input is paired with a regular I/O. Note, the global I/O pads do not need to feed the global network; they can also be used as regular I/O pads.
3 – SRAM and FIFO

Introduction

This section provides an overview of the embedded SRAM and FIFO features of the FPGA fabric within the SmartFusion™ device. This section does not discuss the embedded memory elements (eSRAM) associated with the SmartFusion microcontroller subsystem (MSS). Refer to the appropriate datasheet chapters for a description of the MSS memory features and usage.

SRAM

The SmartFusion FPGA fabric has SRAM blocks along the north side of the die. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks can be independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The SmartFusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 3-1 on page 22 for more information about the implementation of the embedded FIFO controller.

The SmartFusion architecture enables the read and write data widths of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different depth × width or D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 3-1 on page 24.

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.
Figure 3-1 shows a SmartFusion RAM block with an embedded FIFO controller.

Figure 3-1 • SmartFusion RAM Block with Embedded FIFO Controller
RAM4K9 Description

Figure 3-2 • RAM4K9
The following signals are used to configure the RAM4K9 memory element:

**WIDTHA and WIDTHB**
These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 3-1).

<table>
<thead>
<tr>
<th>WIDTHA1, WIDTHA0</th>
<th>WIDTHB1, WIDTHB0</th>
<th>D×W</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>4k×1</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>2k×2</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>1k×4</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>512×9</td>
</tr>
</tbody>
</table>

*Note:* The aspect ratio settings are constant and cannot be changed on the fly.

**BLKA and BLKB**
These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the associated port's outputs hold the previous value.

**WENA and WENB**
These signals switch the RAM between read and write mode for the respective ports. A LOW on these signals indicates a write operation, and a HIGH indicates a read.

**CLKA and CLKB**
These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

**PIPEA and PIPEB**
These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the corresponding output in the next clock cycle.

**WMODEA and WMODEB**
These signals are used to configure the behavior of the output when the RAM is in write mode. A LOW on these signals makes the output retain data from the previous read. A HIGH indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

**RESET**
This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.
ADDRA and ADDRB
These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 3-2).

Table 3-2 • Address Pins Unused/Used for Various Supported Bus Widths

<table>
<thead>
<tr>
<th>D×W</th>
<th>ADDRx</th>
<th>Unused</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>4k×1</td>
<td>None</td>
<td>[11:0]</td>
<td></td>
</tr>
<tr>
<td>2k×2</td>
<td>[11]</td>
<td>[10:0]</td>
<td></td>
</tr>
<tr>
<td>1k×4</td>
<td>[11:10]</td>
<td>[9:0]</td>
<td></td>
</tr>
<tr>
<td>512×9</td>
<td>[11:9]</td>
<td>[8:0]</td>
<td></td>
</tr>
</tbody>
</table>

*Note:* The "x" in ADDRx implies A or B.

DINA and DINB
These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 3-3).

DOUTA and DOUTB
These are the nine bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 3-3). The output data on unused pins is undefined.

Table 3-3 • Unused/Used Input and Output Data Pins for Various Supported Bus Widths

<table>
<thead>
<tr>
<th>D×W</th>
<th>DINx/DOUTx</th>
<th>Unused</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>4k×1</td>
<td>[8:1]</td>
<td>[8:1]</td>
<td>[0]</td>
</tr>
<tr>
<td>2k×2</td>
<td>[8:2]</td>
<td>[8:2]</td>
<td>[1:0]</td>
</tr>
<tr>
<td>1k×4</td>
<td>[8:4]</td>
<td>[8:4]</td>
<td>[3:0]</td>
</tr>
<tr>
<td>512×9</td>
<td>None</td>
<td>None</td>
<td>[8:0]</td>
</tr>
</tbody>
</table>

*Note:* The "x" in DINx and DOUTx implies A or B.
RAM512X18 Description

Figure 3-3 • RAM512X18
RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

**WW and RW**
These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 3-4).

<table>
<thead>
<tr>
<th>WW[1:0]</th>
<th>RW[1:0]</th>
<th>D×W</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>01</td>
<td>512×9</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>256×18</td>
</tr>
<tr>
<td>00, 11</td>
<td>00, 11</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**WD and RD**
These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

**WADDR and RADDR**
These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

**WCLK and RCLK**
These signals are the write and read clocks, respectively. They are both active high.

**WEN and REN**
These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

**RESET**
This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory array.

**PIPE**
This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

**Clocking**
The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks.

SmartFusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK. If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the SmartFusion development tools, without performance penalty.
**Modes of Operation**

There are two read modes and one write mode:

- **Read Nonpipelined (synchronous—1 clock edge):** In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.

- **Read Pipelined (synchronous—2 clock edges):** The pipelined mode incurs an additional clock delay from the address to the data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.

- **Write (synchronous—1 clock edge):** On the write clock active edge, the write data is written into the SRAM at the write address when WEN is HIGH. The setup times of the write address, write enables, and write data are minimal with respect to the write clock.

**RAM Initialization**

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG macro. The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.
FIFO

FIFO4K18 Description

Figure 3-4  FIFO4KX18
The following signals are used to configure the FIFO4K18 memory element:

**WW and RW**
These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 3-5).

*Table 3-5 • Aspect Ratio Settings for WW[2:0]*

<table>
<thead>
<tr>
<th>WW2, WW1, WW0</th>
<th>RW2, RW1, RW0</th>
<th>D×W</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>000</td>
<td>4k×1</td>
</tr>
<tr>
<td>001</td>
<td>001</td>
<td>2k×2</td>
</tr>
<tr>
<td>010</td>
<td>010</td>
<td>1k×4</td>
</tr>
<tr>
<td>011</td>
<td>011</td>
<td>512×9</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>256×18</td>
</tr>
<tr>
<td>101, 110, 111</td>
<td>101, 110, 111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**WBLK and RBLK**
These signals are active low and will enable the respective ports when LOW. When the RBLK signal is HIGH, the corresponding port’s outputs hold the previous value.

**WEN and REN**
Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

**WCLK and RCLK**
These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

**RPIPE**
This signal is used to specify pipelined read on the output. A LOW on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

**RESET**
This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins LOW, the FULL and AFULL pins LOW, and the EMPTY and AEMPTY pins HIGH.

**WD**
This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused most significant bits (MSBs) must be grounded (Table 3-6).

*Table 3-6 • Input Data Signal Usage for Different Aspect Ratios*

<table>
<thead>
<tr>
<th>D×W</th>
<th>WD/RD Unused</th>
</tr>
</thead>
<tbody>
<tr>
<td>4k×1</td>
<td>WD[17:1], RD[17:1]</td>
</tr>
<tr>
<td>2k×2</td>
<td>WD[17:2], RD[17:2]</td>
</tr>
<tr>
<td>1k×4</td>
<td>WD[17:4], RD[17:4]</td>
</tr>
<tr>
<td>512×9</td>
<td>WD[17:9], RD[17:9]</td>
</tr>
<tr>
<td>256×18</td>
<td>–</td>
</tr>
</tbody>
</table>
**RD**

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. As with the WD bus, the MSBs become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 3-6 on page 30.)

**ESTOP, FSTOP**

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes HIGH). A HIGH on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes HIGH). A HIGH on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section.

**FULL, EMPTY**

When the FIFO is full, no more data can be written and the FULL flag asserts HIGH. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts HIGH. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section.

**AFULL, AEMPTY**

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go HIGH. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go HIGH.

**AFVAL, AEVAL**

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section.

**ESTOP and FSTOP Usage**

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes HIGH). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes HIGH).

The FIFO counters in the SmartFusion device start the count at 0, reach the maximum depth for the configuration (511 for a 512×9 configuration, for example), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

**FIFO Flag Usage Considerations**

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address
exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1,500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid half-words being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

For the FPGA core embedded FIFO timing characteristics, refer to the DC and AC specifications section of the SmartFusion Intelligent Mixed-Signal FPGAs datasheet.
4 – SmartFusion FPGA User I/Os

Introduction

This section provides an overview of the digital user I/Os dedicated to the SmartFusion™ FPGA fabric. The SmartFusion device also contains I/Os which are dedicated to the microcontroller subsystem (MSS) and I/Os which are part of the analog system. Additionally, some of the FPGA fabric I/Os can be configured to act as an external memory controller (EMC) interface to the MSS.

SmartFusion devices feature a flexible I/O structure that supports a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Additionally, the FPGA user I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 5 V input tolerance can be achieved with some minimal external circuitry, as described in the "5 V Input Tolerance" section on page 41. Furthermore, 3.3 V LVTTL outputs are directly compatible with 5 V TTL inputs used on external devices.

All I/Os are in a known state during power-up and any power sequence is allowed. When the Digital FPGA user I/Os are not implemented in the user FPGA design, they are tristated.

SmartFusion FPGA fabric I/Os do not inherently support hot-insertion or cold-sparing, since the I/O VCCFPGAIOBx clamp diode is always connected to VCCFPGAIOBx. Refer to the "Cold-Sparing" section on page 39 and the "Electrostatic Discharge (ESD) Protection" section on page 40 for more information.

In addition, the registers available in the SmartFusion FPGA digital I/O tile can be used to support high-performance registered inputs and outputs, with register enable if desired, as described later in this section. The registers can also be used to support the JESD-79C DDR standard within the I/O structure, as described in the "Double Data Rate (DDR) Support" section on page 38.

For I/O and global pin naming and assignments to specific I/O banks, refer to the "Pin Descriptions" section in the SmartFusion Intelligent Mixed-Signal FPGAs datasheet.

![Figure 4-1: SmartFusion A2F200 I/O Bank Location and Naming]
**I/O Banks and I/O Standards Compatibility**

The SmartFusion FPGA digital I/Os are grouped into I/O voltage banks. Figure 4-1 on page 33 shows the I/O bank configuration for the A2F200 device. Each I/O bank has dedicated I/O supply (VCCFPGAIOBx) and ground voltages (GNDQ for input buffers and GND for output buffers). The dedicated voltage supplies mean that only I/Os with compatible standards can be assigned to the same I/O voltage bank. I/O standards are compatible if their VCCFPGAIOBx values are identical. Refer to Table 4-1 for a list of the I/O standards supported on the FPGA fabric I/Os. Additionally, Table 4-2 lists compatible I/O standards for a given VCCFPGAIOBx voltage.

**Table 4-1 • I/O Standards Supported on FPGA I/O Banks**

<table>
<thead>
<tr>
<th>I/O Bank</th>
<th>Single-Ended I/O Standards</th>
<th>Differential I/O Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 0 – North core</td>
<td>LVTTL / LVCMOS 3.3 V</td>
<td>LVPECL</td>
</tr>
<tr>
<td>Bank 1 – East core</td>
<td>LVCMOS 2.5 V / 1.8 V / 1.5 V</td>
<td>LVDS (extendable to B-LVDS and M-LVDS)</td>
</tr>
<tr>
<td>Bank 5 – West core</td>
<td>LVCMOS 2.5/5.0 V</td>
<td></td>
</tr>
<tr>
<td>and EMC</td>
<td>3.3 V PCI / 3.3 V PCI-X</td>
<td></td>
</tr>
</tbody>
</table>

*Note: Bank 2 and Bank 4 belong to the MSS I/Os; Bank 3 is analog I/Os.*

**Table 4-2 • SmartFusion VCCFPGAIOBx Voltages and Compatible Standards**

<table>
<thead>
<tr>
<th>VCCFPGAIOBx (Typical)</th>
<th>Compatible Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td>LVTTL/LVCMOS 3.3 V, PCI 3.3 V / PCI-X 3.3 V, LVPECL</td>
</tr>
<tr>
<td>2.5 V</td>
<td>LVCMOS 2.5 V, LVCMOS 2.5 / 5.0 V, LVDS</td>
</tr>
<tr>
<td>1.8 V</td>
<td>LVCMOS 1.8 V</td>
</tr>
<tr>
<td>1.5 V</td>
<td>LVCMOS 1.5 V</td>
</tr>
</tbody>
</table>
Features Supported on All Digital FPGA User I/Os

Table 4-3 lists all features supported by the transmitter and receiver for single-ended and differential I/Os.

Table 4-3 • SmartFusion FPGA Fabric I/O Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended transmitter features</td>
<td>• Weak pull-up and pull-down</td>
</tr>
<tr>
<td></td>
<td>• Two slew rates (Low, High)</td>
</tr>
<tr>
<td></td>
<td>• Five drive strengths (2 mA, 4 mA, 8 mA, 16 mA, and 24 mA)</td>
</tr>
<tr>
<td></td>
<td>• Skew between output buffer enable/disable time: 1.2 ns delay (rising edge)</td>
</tr>
<tr>
<td></td>
<td>• Skew between output buffer enable/disable time: 0 ns delay (falling edge); see Table 4-7 on page 46 for more information</td>
</tr>
<tr>
<td></td>
<td>• LVTT/LVCMOS 3.3 V outputs compatible with external 5 V TTL inputs (see “5 V Output Tolerance” section on page 46)</td>
</tr>
<tr>
<td></td>
<td>• High performance (Table 4-5 on page 36)</td>
</tr>
<tr>
<td>Single-ended receiver features</td>
<td>• 5 V tolerant with use of minimal external circuitry</td>
</tr>
<tr>
<td></td>
<td>• ESD protection</td>
</tr>
<tr>
<td></td>
<td>• High performance (Table 4-5 on page 36)</td>
</tr>
<tr>
<td></td>
<td>• Separate ground planes, GND/GNDQ for input and output buffers to avoid output-induced noise in the input circuitry</td>
</tr>
<tr>
<td>CMOS-style LVDS or LVPECL transmitter</td>
<td>• Two I/Os and external resistors are used to provide a CMOS-style LVDS or LVPECL transmitter solution</td>
</tr>
<tr>
<td></td>
<td>• LVDS transmitter solution can also support bus LVDS (B-LVDS) and multipoint LVDS (M-LVDS)</td>
</tr>
<tr>
<td></td>
<td>• Weak pull-up and pull-down</td>
</tr>
<tr>
<td></td>
<td>• Fast slew rate</td>
</tr>
<tr>
<td>LVDS/LVPECL differential receiver</td>
<td>• ESD protection</td>
</tr>
<tr>
<td></td>
<td>• High performance (Table 4-5 on page 36)</td>
</tr>
<tr>
<td></td>
<td>• Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry</td>
</tr>
</tbody>
</table>
**Multiplexed I/Os Used for FPGA Fabric and External Memory Controller (EMC) Interface**

Some of the SmartFusion FPGA fabric user I/Os are shared between the FPGA fabric and the microcontroller subsystem's (MSS) external memory controller (EMC). These multiplexed I/O pins can be configured to act as an external memory controller (EMC), enabling the ARM® Cortex™-M3 processor to seamlessly interface to standard external memory chips via the internal EMC.

When the EMC is used, those I/O pins are no longer available to act as FPGA fabric I/Os. This means that user I/O signals must be placed on other available FPGA fabric I/Os. When the EMC is used, a total of 50 FPGA fabric I/Os will be dedicated to the EMC and are no longer available to user FPGA I/O signals. The EMC signals implement external memory control and data signals including a memory clock, read/write enables, chip selects, memory address and data buses. The multiplexed I/Os are located on North I/O Bank 0 (for EMC address and control signals) and West I/O Bank 5 (for EMC Data signals) as shown in Figure 4-1 on page 33. To determine the specific pins which are used for the EMC, refer to the "Pin Assignment Tables" section in the *SmartFusion Intelligent Mixed-Signal FPGAs* datasheet for the specific device package in use.

The pins will be identified in the format shown below:

- EMC_xxxx / IOuxwBy

When the EMC shares a global User I/O pin, the format matches the example below:

- EMC_CLK / Gmn / IOuxwBy

Note that the I/O configuration is set when the SmartFusion FPGA is programmed. I/Os configured as EMC I/Os have their configuration fixed as shown in Table 4-4.

### Table 4-4 • I/O Standard and Attribute Fixed Configuration of EMC I/Os

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>SLEW (output only)</th>
<th>OUT_DRIVE (output only)</th>
<th>SKEW (TRIBUF and BIBUF macros with OE)</th>
<th>RES_PULL</th>
<th>COMBINE_REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL/LVCMOS 3.3V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>–</td>
</tr>
</tbody>
</table>

### Table 4-5 • Maximum I/O Frequency for Single-Ended and Differential I/Os

(maximum drive strength and high slew rate selected)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Performance Up To</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL/LVCMOS 3.3 V</td>
<td>200 MHz</td>
</tr>
<tr>
<td>LVCMOS 2.5 V</td>
<td>250 MHz</td>
</tr>
<tr>
<td>LVCMOS 1.8 V</td>
<td>200 MHz</td>
</tr>
<tr>
<td>LVCMOS 1.5 V</td>
<td>130 MHz</td>
</tr>
<tr>
<td>PCI</td>
<td>200 MHz</td>
</tr>
<tr>
<td>PCI-X</td>
<td>200 MHz</td>
</tr>
<tr>
<td>LVDS</td>
<td>350 MHz</td>
</tr>
<tr>
<td>LVPECL</td>
<td>300 MHz</td>
</tr>
</tbody>
</table>
I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 4-2 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 4-2) between registers to implement single or differential data transmission to and from the FPGA fabric. The Designer software sets these switches for the user.

A common CLR/PRE signal is used by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, because this register is used for DDR implementation. The I/O register combining must satisfy specific design rules described in the Designer software documentation and online help.

Note: SmartFusion I/Os have registers to support DDR functionality (see the “Double Data Rate (DDR) Support” section on page 38 for more information).

Figure 4-2 • I/O Block Logical Representation
Double Data Rate (DDR) Support

SmartFusion I/Os support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every edge of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making it very efficient for implementing very high-speed systems.

DDR interfaces can be implemented using LVDS and LVPECL I/O standards. In addition, high-speed DDR interfaces can be implemented using LVDS I/O.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 4-3. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock. Each FPGA fabric I/O tile on SmartFusion devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 4-4 on page 39. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The Designer Compile tool automatically recognizes the DDR macro and maps its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

Figure 4-3 • DDR Input Register Support in SmartFusion Devices
Cold-Sparing

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

While it is true that the SmartFusion FPGA fabric I/Os are tristated when there is no power applied to the device, there is an I/O VCCFPGAIOBx clamp diode that is always connected to VCCFPGAIOBx. In normal DC operating conditions, the I/O pad voltage will not exceed the VCCFPGAIOBx supply voltage and the clamp diode will not be forward-biased. However, in a cold-sparing scenario when VCCFPGAIOBx is not powered (0 V) and a DC voltage is placed on the I/O pad (>0 V), this will forward bias the clamp diode and result in a potentially high current powering up the VCCFPGAIOBx plane. This situation can potentially damage the I/O pin, since it exceeds the recommended DC operating conditions.

If cold-sparing is required, it can be accomplished either by using an external bus switch to isolate the device I/Os from the rest of the system or by driving each FPGA fabric I/O pin to 0 V.

Hot-Swap

Hot-swapping (also called hot-plugging) is the operation of hot insertion (or hot removal) of a card in (or from) a powered-up system.

SmartFusion FPGA fabric I/Os do not inherently support hot-swap since the VCCFPGAIOBx clamp diode is always enabled, as described in the “Cold-Sparing” section.

However, if external circuitry such as an external bus switch is used to isolate the device I/Os from the rest of the system, a cold-swap or a hot-swap while in reset might be possible if certain considerations are made.
A cold-swap implies that a system and card with a SmartFusion device are powered down before the card is inserted into the system. Card insertion is followed by the system power-up while the card supplies remain off. In this scenario, if the SmartFusion fabric I/Os are isolated from the card and system via external circuitry such as a bus switch, this will ensure that the fabric I/Os are not driven while the VCCFPGAIOBx is not powered.

A hot-swap while in reset implies that the card containing the SmartFusion device is inserted into a powered system which is holding the card buses in reset until the card power supplies are at their nominal operating levels and are stable. Again, if the card designer ensures that the SmartFusion fabric I/Os are not driven before the SmartFusion VCCFPGAIOBx power supply is applied, this type of operation is possible. This implies fabric I/O isolation via a bus switch and an appropriate card connection power-up sequence, such as grounds, then power supplies, then I/Os, etc.

**Electrostatic Discharge (ESD) Protection**

SmartFusion devices are tested per JEDEC Standard JESD22-A114-B.

SmartFusion devices contain clamp diodes at every FPGA fabric I/O, global, and power pad. Clamp diodes protect device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes:

- One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCFPGAIOBx. This is also referred to as the power clamp or the VCCFPGAIOBx clamp diode.

- The second diode has its P side connected to GND and its N side connected to the pad. This is also referred to as the GND clamp.

During operation, these diodes are normally biased in the OFF state, except when transient voltage is significantly above VCCFPGAIOBx or below GND levels.

On SmartFusion FPGA fabric I/Os, each power and ground clamp diode is always connected to VCCFPGAIOBx and GND, respectively.
5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V / 5 V, and LVCMOS 2.5 V configurations are used (see Table 4-6 on page 45 for more details). There are four recommended solutions (see Figure 4-5 on page 42 to Figure 4-8 on page 44 for details of board and macro setups) to achieve 5 V receiver tolerance. All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design needs to ensure that the reflected waveform at the pad does not exceed limits. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI / PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors, as described below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

The following are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where $R_{tx\_out\_high} = (V_{CC\_FPGA\_IOBx} - V_{OH}) / I_{OH}$, $R_{tx\_out\_low} = V_{OL} / I_{OL}$).

Example 1 (high speed, high current):

<table>
<thead>
<tr>
<th>$R_{tx_out_high}$</th>
<th>$R_{tx_out_low}$</th>
<th>$R_{ext1}$</th>
<th>$R_{ext2}$</th>
<th>$I_{max_tx}$</th>
<th>$t_{RISE} = t_{FALL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Ω</td>
<td>10 Ω</td>
<td>36 Ω (±5%)</td>
<td>82 Ω (±5%)</td>
<td>45.04 mA</td>
<td>0.85 ns at $C_{pad_load} = 10$ pF (includes up to 25% safety margin)</td>
</tr>
</tbody>
</table>

$t_{RISE} = t_{FALL} = 4$ ns at $C_{pad\_load} = 50$ pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

<table>
<thead>
<tr>
<th>$R_{tx_out_high}$</th>
<th>$R_{tx_out_low}$</th>
<th>$R_{ext1}$</th>
<th>$R_{ext2}$</th>
<th>$I_{max_tx}$</th>
<th>$t_{RISE} = t_{FALL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Ω</td>
<td>10 Ω</td>
<td>220 Ω (±5%)</td>
<td>390 Ω (±5%)</td>
<td>9.17 mA</td>
<td>4 ns at $C_{pad_load} = 10$ pF (includes up to 25% safety margin)</td>
</tr>
</tbody>
</table>

$t_{RISE} = t_{FALL} = 20$ ns at $C_{pad\_load} = 50$ pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to $2.5 V < V_{in\_rx} < 3.6 V$ when the transmitter sends a logic 1. This
range of $V_{\text{in,dc}}(\text{rx})$ must be assured for any combination of transmitter supply ($5 \text{ V} \pm 0.5 \text{ V}$), transmitter output resistance, and board resistor tolerances.

---

**Solution 1**

![Diagram of Solution 1](image)

- **Off-Chip**:
  - 5.5 V
  - Rext1
  - Rext2

- **On-Chip**:
  - 3.3 V

Requires two board resistors, LVCMOS 3.3 V I/Os

---

*Figure 4-5 • Solution 1*
Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should be turned off and not used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 4-6. Relying on the diode clamping would create an excessive pad DC voltage of $3.3\, \text{V} + 0.7\, \text{V} = 4\, \text{V}$.

![Figure 4-6 • Solution 2](image)

Solution 2

- Requires one board resistor, one Zener 3.3 V diode, LVCMOS 3.3 V I/Os
**Solution 3**

The board-level design must ensure that the reflected waveform at the pad does not exceed limits. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 4-7. Relying on the diode clamping would create an excessive pad DC voltage of $3.3\,\text{V} + 0.7\,\text{V} = 4\,\text{V}$.

---

**Solution 3**

![Solution 3 Diagram](image)

Requires a bus switch on the board, LVTTL/LVCMOS 3.3 V I/Os.

---

**Solution 4**

---

**Solution 4**

![Solution 4 Diagram](image)

Requires one board resistor. Available for LVCMOS 2.5 V / 5.0 V.
### Table 4-6 • Comparison Table for 5 V Compliant Receiver Scheme

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Board Components</th>
<th>Speed</th>
<th>Current Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Two resistors</td>
<td>Low to high&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Limited by transmitter's drive strength</td>
</tr>
<tr>
<td>2</td>
<td>Resistor and Zener 3.3 V</td>
<td>Medium</td>
<td>Limited by transmitter's drive strength</td>
</tr>
<tr>
<td>3</td>
<td>Bus switch</td>
<td>High</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>Minimum resistor value&lt;sup&gt;2&lt;/sup&gt; (R = 47 , \Omega) at (T_J = 70°C) (R = 150 , \Omega) at (T_J = 85°C) (R = 420 , \Omega) at (T_J = 100°C)</td>
<td>Medium</td>
<td>Maximum diode current at 100% duty cycle, signal constantly at 1. (52.7 , mA) at (T_J = 70°C); (16.5 , mA) at (T_J = 85°C); (5.9 , mA) at (T_J = 100°C); For duty cycles other than 100%, the currents can be increased by a factor = 1 / (duty cycle). Example: 20% duty cycle at 70°C, maximum current = ((1 / 0.2) \times 52.7 , mA = 5 \times 52.7 , mA = 263.5 , mA)</td>
</tr>
</tbody>
</table>

**Notes:**

1. Speed and current consumption increase as the board resistance values decrease.
2. Resistor values must ensure I/O diode long-term reliability.
5 V Output Tolerance

SmartFusion I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, SmartFusion I/Os can directly drive signals into 5 V TTL receivers. In fact, $V_{OL} = 0.4$ V and $V_{OH} = 2.4$ V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceed the $V_{IL} = 0.8$ V and $V_{IH} = 2$ V level requirements of 5 V TTL receivers. Therefore, logic level 1 and logic level 0 will be correctly recognized by 5 V TTL receivers.

Table 4-7 • Summary of SmartFusion Hot-Insertion, Cold-Sparing and 5 V Input Tolerance Capabilities

<table>
<thead>
<tr>
<th>I/O Assignment</th>
<th>Clamp Diode</th>
<th>Hot-Insertion</th>
<th>Cold-Sparing</th>
<th>5 V Input Tolerance</th>
<th>Input Buffer</th>
<th>Output Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V LVTTL/LVCMOS</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes$^1$</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>3.3 V PCI / PCI-X</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes$^1$</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>LVCMOS 2.5 V</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes$^2$</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>LVCMOS 2.5 / 5.0 V</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes$^2$</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>LVCMOS 1.8 V</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>LVCMOS 1.5 V</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
<tr>
<td>LVDS and LVPECL$^3$</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Enabled/Disabled</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.
2. Can be implemented with an external resistor and an internal clamp diode.
3. Bidirectional LVPECL buffers are not supported. I/Os can be configured as either input buffers or output buffers.

Simultaneously Switching Outputs and PCB Layout

- Simultaneously switching outputs (SSOs) can impact the signal integrity of adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO buses onto signals adjacent to those buses. Additionally, SSOs can produce ground bounce noise and VCCFPGAIOBx dip noise. These two noise types are caused by rapidly changing currents through GND and VCCFPGAIOBx package pin inductances during switching activities:
  - Ground bounce noise voltage = $L(GND) \times \frac{di}{dt}$
  - VCCFPGAIOBx dip noise voltage = $L(VCCFPGAIOBx) \times \frac{di}{dt}$

Any group of four or more output pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to the SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus must be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to be considered are as follows:
- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations
Selectable Skew between Output Buffer Enable/Disable Time

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

---

**Figure 4-9 • Block Diagram of Output Enable Path**

---

**Figure 4-10 • Timing Diagram (option 1: bypasses skew circuit)**

---

**Figure 4-11 • Timing Diagram (option 2: enables skew circuit)**
At the system level, the enable skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. When selected, this circuit provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 4-12 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 4-13 shows how bus contention is created, and Figure 4-14 on page 49 shows how it can be avoided with the skew circuit.

Figure 4-12 • Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using SmartFusion Devices

Figure 4-13 • Timing Diagram (bypasses skew circuit)
Weak Pull-Up and Weak Pull-Down Resistors

SmartFusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCFPGAIOBx of its corresponding I/O bank. When it is pulled down, it is connected to GND.

Slew Rate Control and Drive Strength

SmartFusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVC莫斯 3.3 V, LVC莫斯 2.5 V, LVC莫斯 2.5 V / 5.0 V input, LVC莫斯 1.8 V, and LVC莫斯 1.5 V. All differential I/O standards have a high output slew rate by default. Furthermore, 3.3 V PCI / PCI-X I/O standards have a low output slew rate by default.

For SmartFusion FPGA fabric I/O slew rate and drive strength specifications, refer to Table 4-8 on page 50. Note that fabric I/Os being used as EMC I/Os will have a fixed I/O standard and attribute configuration, as shown on Table 4-4 on page 36. Low slew and low drive strength are recommended in the case of a large SSO bus toggling at high frequency.
I/O Software Support

In the SmartFusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes. Note that not all I/O attributes are applicable for all I/O standards. Table 4-9 lists the valid I/O attributes that can be manipulated by the user for each I/O standard. Table 4-10 on page 51 lists the default software I/O attribute configuration.

Table 4-9 • SmartFusion FPGA Fabric I/O Configurable I/O Attributes

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>SLEW (output only)</th>
<th>OUT_DRIVE (output only)</th>
<th>SKEW (TRIBUF and BIBUF macros with OE)</th>
<th>RES_PULL</th>
<th>OUT_LOAD (output only)</th>
<th>COMBINE_REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL/LVCMOS 3.3 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LVCMOS 2.5 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LVCMOS 2.5 / 5.0 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LVCMOS 1.8 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LVCMOS 1.5 V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LVDS, LVPECL</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>✓</td>
</tr>
<tr>
<td>3.3 V PCI / PCI-X</td>
<td>–</td>
<td>–</td>
<td>✓</td>
<td>–</td>
<td>–</td>
<td>✓</td>
</tr>
</tbody>
</table>
### Table 4-10 • FPGA Fabric I/O Default Attribute Configuration in Software

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>SLEW (output only)</th>
<th>OUT_DRIVE (output only)</th>
<th>SKEW (TRIBUF and BIBUF macros with OE)</th>
<th>RES_PULL</th>
<th>OUT_LOAD (output only)</th>
<th>COMBINE_REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVTTL/LVC莫斯 3.3 V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>35 pF</td>
<td>–</td>
</tr>
<tr>
<td>LVCMOS 2.5 V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>35 pF</td>
<td>–</td>
</tr>
<tr>
<td>LVCMOS 2.5 / 5.0 V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>35 pF</td>
<td>–</td>
</tr>
<tr>
<td>LVCMOS 1.8 V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>35 pF</td>
<td>–</td>
</tr>
<tr>
<td>LVCMOS 1.5 V</td>
<td>High</td>
<td>12 mA</td>
<td>Off</td>
<td>None</td>
<td>35 pF</td>
<td>–</td>
</tr>
<tr>
<td>LVDS</td>
<td>High</td>
<td>24 mA</td>
<td>Off</td>
<td>None</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>LVPECL</td>
<td>High</td>
<td>24 mA</td>
<td>Off</td>
<td>None</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>3.3 V PCI / PCI-X</td>
<td>Low</td>
<td>PCI Setting</td>
<td>Off</td>
<td>None</td>
<td>10 pF</td>
<td>–</td>
</tr>
</tbody>
</table>
The following table lists critical changes that were made in the current version of the SmartFusion FPGA Fabric User’s Guide.

<table>
<thead>
<tr>
<th>Previous Version</th>
<th>Changes in Current Version (Revision 0)</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Draft B (December 2009)</td>
<td>A note was added to Table 1-1 • Array Coordinates, accounting for Banks 2, 3, and 4.</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>OUT_LOAD was removed from Table 4-4 • I/O Standard and Attribute Fixed Configuration of EMC I/Os.</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>The &quot;Simultaneously Switching Outputs and PCB Layout&quot; section was revised.</td>
<td>46</td>
</tr>
<tr>
<td>Draft A (September 2009)</td>
<td>The &quot;VersaTile&quot; section was revised.</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>EMI was changed to EMC in Figure 4-1 • SmartFusion A2F200 I/O Bank Location and Naming.</td>
<td>33</td>
</tr>
</tbody>
</table>
Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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- From Southeast and Southwest U.S.A., call **650.318.4480**
- From South Central U.S.A., call **650.318.4434**
- From Northwest U.S.A., call **650.318.4434**
- From Canada, call **650.318.4480**
- From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
- From Japan, call **650.318.4743**
- From the rest of the world, call **650.318.4743**
- Fax, from anywhere in the world **650.318.8044**

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The technical support email address is tech@actel.com.

**Phone**

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- 650.318.4460
- 800.262.1060

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