Announcements

• Extra open labs
  – Friday 2 - 4pm or Saturday 12-2pm
  – Monday 9:30 - 11:30am

• Lab 3: IO Attribute Editor Problems
  – From Andrzej K.:
    I noticed another problem with Libero and Lab 3. When the IO Attributes Editor comes up, sometimes the listed port names do not match the ones referred to in the schematic and Lab 1. To fix this problem I went back to "Design Hierarchy " right clicked on "lab3fpga_MSS_0" and selected "set as root". Then Generate Component and Synthesize again. This updated the IO editor with the correct port names.

• Late labs...
Using the EMC to attach two S29GL512’s

- $2^{26} \times 8 = 64$ MByte
- EMC_AB[0] = 0
- We loose half the memory!

From Microsemi MSS User Guide
Minute Quiz
Interrupts

Merriam-Webster:
- “to break the uniformity or continuity of”

- Informs a program of some external events
- Breaks execution flow

Key questions:
- Where do interrupts come from?
- How do we save state for later continuation?
- How can we ignore interrupts?
- How can we prioritize interrupts?
- How can we share interrupts?
Two key questions to determine how data is transferred to/from a non-trivial I/O device:

1. How does the CPU know when data is available?
   a. Polling
   b. Interrupts

2. How is data transferred into and out of the device?
   a. Programmed I/O
   b. Direct Memory Access (DMA)
Interrupt (a.k.a. exception or trap):
• An event that causes the CPU to stop executing the current program and begin executing a special piece of code called an **interrupt handler** or **interrupt service routine** (ISR). Typically, the ISR does some work and then resumes the interrupted program.

Interrupts are really glorified procedure calls, except that they:
• **can occur between any two instructions**
• are transparent to the running program (usually)
• are not explicitly requested by the program (typically)
• call a procedure at an address determined by the type of interrupt, not the program
Two basic types of interrupts (1/2)

• Those caused by an instruction
  - Examples:
    • TLB miss
    • Illegal/unimplemented instruction
    • div by 0
  - Names:
    • Trap, exception
Two basic types of interrupts (2/2)

• Those caused by the external world
  - External device
  - Reset button
  - Timer expires
  - Power failure
  - System error

• Names:
  - interrupt, external interrupt
How it works

• Something tells the processor core there is an interrupt
• Core transfers control to code that needs to be executed
• Said code “returns” to old program
• Much harder then it looks.
  - Why?
... is in the details

- How do you figure out where to branch to?
- How do you ensure that you can get back to where you started?
- Don’t we have a pipeline? What about partially executed instructions?
- What if we get an interrupt while we are processing our interrupt?
- What if we are in a “critical section?”
The Cortex-M3 processor has a three-stage pipeline. The pipeline stages are instruction fetch, instruction decode, and instruction execution (see Figure 6.1).

Some people might argue that there are four stages because of the pipeline behavior in the bus interface when it accesses memory, but this stage is outside the processor, so the processor itself still has only three stages.

When running programs with mostly 16-bit instructions, you will find that the processor might not fetch instructions in every cycle. This is because the processor fetches up to two instructions (32-bit) in one go, so after one instruction is fetched, the next one is already inside the processor. In this case, the processor bus interface may try to fetch the instruction after the next or, if the buffer is full, the bus interface could be idle. Some of the instructions take multiple cycles to execute; in this case, the pipeline will be stalled.

In executing a branch instruction, the pipeline will be flushed. The processor will have to fetch instructions from the branch destination to fill up the pipeline again. However, the Cortex-M3 processor supports a number of instructions in v7-M architecture, so some of the short-distance branches can be avoided by replacing them with conditional execution codes.

Due to the pipeline nature of the processor and to ensure that the program is compatible with Thumb codes, when the program counter is read during instruction execution, the read value will be the address of the instruction plus 4. This offset is constant, independent of the combination of 16-bit Thumb instructions and 32-bit Thumb-2 instructions. This ensures consistency between Thumb and Thumb-2.

Inside the instruction pre-fetch unit of the processor core, there is also an instruction buffer. This buffer allows additional instructions to be queued before they are needed. This buffer prevents the pipeline being stalled when the instruction sequence contains 32-bit Thumb-2 instructions that are not word aligned. However, this buffer does not add an extra stage to the pipeline, so it does not increase the branch penalty.
• If you know *what* caused the interrupt then you want to jump to the code that handles that interrupt.
  - If you number the possible interrupt cases, and an interrupt comes in, you can just branch to a location, using that number as an offset (this is a branch table)
  - If you don’t have the number, you need to *poll* all possible sources of the interrupt to see who caused it.
    • Then you branch to the right code
• Need to store the return address somewhere.
  - Stack *might* be a scary place.
    • *That* would involve a load/store and might cause an interrupt (page fault)!
  - So a dedicated register seems like a good choice
    • But that might cause problems later…
Snazzy architectures

• A modern processor has *many* (often 50+) instructions in-flight at once.
  - What do we do with them?
• Drain the pipeline?
  - What if one of them causes an exception?
• Punt all that work
  - Slows us down
Nested interrupts

• If we get one interrupt while handling another what to do?
  - Just handle it
    • But what about that dedicated register?
    • What if I’m doing something that can’t be stopped?
  - Ignore it
    • But what if it is important?
  - Prioritize
    • Take those interrupts you care about. Ignore the rest
    • Still have dedicated register problems.
Critical section

• We probably need to ignore some interrupts but take others.
  - Probably should be sure our code can’t cause an exception.
  - Use same prioritization as before.
1) No power

2) System is held in RESET as long as VCC15 < 0.8V
   a) In reset: registers forced to default
   b) RC-Osc begins to oscillate
   c) MSS_CCC drives RC-Osc/4 into FCLK
   d) PORESET_N is held low

3) Once VCC15GOOD, PORESET_N goes high
   a) MSS reads from eNVM address 0x0 and 0x4
The Reset Interrupt (2)

The Reset Interrupt is Non-Maskable!
The Nested Vectored Interrupt Controller (NVIC) on the Cortex-M3

- Control registers are memory mapped
- Contains control logic for interrupt processing

- 15 internal interrupts (defined by ARM)
- Supports up to 240 external interrupts (vendor specific)
- Accessed at 0xE000E000 on any Cortex-M3!

- Register definitions can be found at:
  - ARM Cortex-M3 Technical Reference Manual v2.1, Chapter 6
  - The Definitive Guide to the ARM Cortex-M3
# System Exceptions

## NVIC Interrupts 1-15

<table>
<thead>
<tr>
<th>Exception Number</th>
<th>Exception Type</th>
<th>Priority</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reset</td>
<td>−3 (Highest)</td>
<td>Reset</td>
</tr>
<tr>
<td>2</td>
<td>NMI</td>
<td>−2</td>
<td>Nonmaskable interrupt (external NMI input)</td>
</tr>
<tr>
<td>3</td>
<td>Hard Fault</td>
<td>−1</td>
<td>All fault conditions, if the corresponding fault handler is not enabled</td>
</tr>
<tr>
<td>4</td>
<td>MemManage Fault</td>
<td>Programmable</td>
<td>Memory management fault; MPU violation or access to illegal locations</td>
</tr>
<tr>
<td>5</td>
<td>Bus Fault</td>
<td>Programmable</td>
<td>Bus error; occurs when AHB interface receives an error response from a bus slave (also called <code>prefetch abort</code> if it is an instruction fetch or <code>data abort</code> if it is a data access)</td>
</tr>
<tr>
<td>6</td>
<td>Usage Fault</td>
<td>Programmable</td>
<td>Exceptions due to program error or trying to access coprocessor (the Cortex-M3 does not support a coprocessor)</td>
</tr>
<tr>
<td>7–10</td>
<td>Reserved</td>
<td>NA</td>
<td>–</td>
</tr>
<tr>
<td>11</td>
<td>SVCALL</td>
<td>Programmable</td>
<td>System Service call</td>
</tr>
<tr>
<td>12</td>
<td>Debug Monitor</td>
<td>Programmable</td>
<td>Debug monitor (breakpoints, watchpoints, or external debug requests)</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
<td>NA</td>
<td>–</td>
</tr>
<tr>
<td>14</td>
<td>PendSV</td>
<td>Programmable</td>
<td>Pendable request for system device</td>
</tr>
<tr>
<td>15</td>
<td>SYSTICK</td>
<td>Programmable</td>
<td>System Tick Timer</td>
</tr>
</tbody>
</table>

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Table 7.1: List of System Exceptions

Table 7.2: List of External Interrupts

From: The Definitive Guide to the ARM Cortex-M3
# SmartFusion Interrupts

<table>
<thead>
<tr>
<th>Cortex-M3 NVIC Input</th>
<th>IRQ Label</th>
<th>IRQ Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMI</td>
<td>WDOGTIMEOUT_IRQ</td>
<td>WATCHDOG</td>
</tr>
<tr>
<td>INTS[0]</td>
<td>WDOGWAKEUP_IRQ</td>
<td>WATCHDOG</td>
</tr>
<tr>
<td>INTS[1]</td>
<td>BROWNOUT1_5V_IRQ</td>
<td>VR/PSM</td>
</tr>
<tr>
<td>INTS[2]</td>
<td>BROWNOUT3_3V_IRQ</td>
<td>VR/PSM</td>
</tr>
<tr>
<td>INTS[3]</td>
<td>RTCMATCHEVENT_IRQ</td>
<td>RTC</td>
</tr>
<tr>
<td>INTS[4]</td>
<td>PU_N_IRQ</td>
<td>RTC</td>
</tr>
<tr>
<td>INTS[5]</td>
<td>EMAC_IRQ</td>
<td>Ethernet MAC</td>
</tr>
<tr>
<td>INTS[7]</td>
<td>ENVM_0_IRQ</td>
<td>ENVM Controller</td>
</tr>
<tr>
<td>INTS[8]</td>
<td>ENVM_1_IRQ</td>
<td>ENVM Controller</td>
</tr>
<tr>
<td>INTS[9]</td>
<td>DMA_IRQ</td>
<td>Peripheral DMA</td>
</tr>
<tr>
<td>INTS[10]</td>
<td>UART_0_IRQ</td>
<td>UART_0</td>
</tr>
<tr>
<td>INTS[11]</td>
<td>UART_1_IRQ</td>
<td>UART_1</td>
</tr>
<tr>
<td>INTS[12]</td>
<td>SPI_0_IRQ</td>
<td>SPI_0</td>
</tr>
<tr>
<td>INTS[13]</td>
<td>SPI_1_IRQ</td>
<td>SPI_1</td>
</tr>
<tr>
<td>INTS[14]</td>
<td>I2C_0_IRQ</td>
<td>I2C_0</td>
</tr>
<tr>
<td>INTS[15]</td>
<td>I2C_0_SMBALET_IRQ</td>
<td>I2C_0</td>
</tr>
<tr>
<td>INTS[16]</td>
<td>I2C_0_SMBSUS_IRQ</td>
<td>I2C_0</td>
</tr>
<tr>
<td>INTS[17]</td>
<td>I2C_1_IRQ</td>
<td>I2C_1</td>
</tr>
<tr>
<td>INTS[18]</td>
<td>I2C_1_SMBALET_IRQ</td>
<td>I2C_1</td>
</tr>
<tr>
<td>INTS[19]</td>
<td>I2C_1_SMBSUS_IRQ</td>
<td>I2C_1</td>
</tr>
<tr>
<td>INTS[20]</td>
<td>TIMER_1_IRQ</td>
<td>TIMER</td>
</tr>
<tr>
<td>INTS[21]</td>
<td>TIMER_2_IRQ</td>
<td>TIMER</td>
</tr>
<tr>
<td>INTS[22]</td>
<td>PLLLOCK_IRQ</td>
<td>MSS_CCC</td>
</tr>
<tr>
<td>INTS[23]</td>
<td>PLLLOCKLOST_IRQ</td>
<td>MSS_CCC</td>
</tr>
<tr>
<td>INTS[24]</td>
<td>ASBM_ERROR_IRQ</td>
<td>AHB BUS MATRIX</td>
</tr>
<tr>
<td>INTS[25]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[26]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[27]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[28]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[29]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[30]</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTS[31]</td>
<td>FAB_IRQ</td>
<td>FABRIC INTERFACE</td>
</tr>
<tr>
<td>INTS[32]</td>
<td>GPIO_0_IRQ</td>
<td>GPIO</td>
</tr>
<tr>
<td>INTS[33]</td>
<td>GPIO_1_IRQ</td>
<td>GPIO</td>
</tr>
<tr>
<td>INTS[34]</td>
<td>GPIO_2_IRQ</td>
<td>GPIO</td>
</tr>
<tr>
<td>INTS[35]</td>
<td>GPIO_3_IRQ</td>
<td>GPIO</td>
</tr>
</tbody>
</table>

54 more ACE specific interrupts

23 GPIO_3_IRQ to GPIO_31_IRQ cut
Pending interrupts

The normal case. Once Interrupt request is seen, processor puts it in “pending” state even if hardware drops the request. IPS is cleared by the hardware once we jump to the ISR.
In this case, the processor never took the interrupt because we cleared the IPS by hand (via a memory-mapped I/O register).
Pending of an interrupt can happen even if the interrupt is disabled; the pended interrupt can then trigger the interrupt sequence when the enable is set later. As a result, before enabling an interrupt, it could be useful to check whether the pending register has been set. The interrupt source might have been activated previously and have set the pending status. If necessary, you can clear the pending status before you enable an interrupt.

![Diagram showing the relationship between Interrupt Request, Pending Status, Active Status, and Handler Mode.](image-url)
Multiple Interrupt Pulses

Pending of an interrupt can happen even if the interrupt is disabled; the pended interrupt can then trigger the interrupt sequence when the enable is set later. As a result, before enabling an interrupt, it could be useful to check whether the pending register has been set. The interrupt source might have been activated previously and have set the pending status. If necessary, you can clear the pending status before you enable an interrupt.

**Figure 7.11 Continuous Interrupt Request Pends Again After Interrupt Exit**

**Figure 7.12 Interrupt Pending Only Once, Even with Multiple Pulses Before the Handler**
New Interrupt Request after Pending Cleared

Exceptions

Fault Exceptions

A number of system exceptions are useful for fault handling. There are several categories of faults:

- Bus faults
- Memory management faults
- Usage faults
- Hard faults

Bus Faults

Bus faults are produced when an error response is received during a transfer on the AHB interfaces. It can happen at these stages:

- Instruction fetch, commonly called prefetch abort
- Data read/write, commonly called data abort

In the Cortex-M3, bus faults can also occur during a:

- Stack PUSH in the beginning of interrupt processing, called a stacking error
- Stack POP at the end of interrupt processing, called an unstacking error

Interrupt Request after Pending Cleared

From: The Definitive Guide to the ARM Cortex-M3
Configuring the NVIC

- **Interrupt Set Enable and Clear Enable**
  - 0xE000E100-0xE000E11C, 0xE000E180-0xE000E19C

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0xE000E100 | SETENA0   | R/W  | 0           | Enable for external interrupt #0–31
  - bit[0] for interrupt #0 (exception #16)
  - bit[1] for interrupt #1 (exception #17)
  - ...
  - bit[31] for interrupt #31 (exception #47)
  - Write 1 to set bit to 1; write 0 has no effect
  - Read value indicates the current status |
| 0xE000E104 | SETENA1   | R/W  | 0           | Clear enable for external interrupt #0–31
  - bit[0] for interrupt #0
  - bit[1] for interrupt #1
  - ...
  - bit[31] for interrupt #31
  - Write 1 to clear bit to 0; write 0 has no effect
  - Read value indicates the current enable status |
| 0xE000E108 | SETENA2   | R/W  | 0           | Clear enable for external interrupt #32–63
  - bit[0] for interrupt #32
  - bit[1] for interrupt #33
  - ...
  - bit[31] for interrupt #63
  - Write 1 to clear bit to 0; write 0 has no effect
  - Read value indicates the current enable status |
| 0xE000E180 | CLRENA0   | R/W  | 0           | Clear enable for external interrupt #64–95
  - bit[0] for interrupt #64
  - bit[1] for interrupt #65
  - ...
  - bit[31] for interrupt #95
  - Write 1 to clear bit to 0; write 0 has no effect
  - Read value indicates the current enable status |
| 0xE000E184 | CLRENA1   | R/W  | 0           | Clear enable for external interrupt #96–127
  - bit[0] for interrupt #96
  - bit[1] for interrupt #97
  - ...
  - bit[31] for interrupt #127
  - Write 1 to clear bit to 0; write 0 has no effect
  - Read value indicates the current enable status |
| 0xE000E188 | CLRENA2   | R/W  | 0           | Clear enable for external interrupt #128–159
  - bit[0] for interrupt #128
  - bit[1] for interrupt #129
  - ...
  - bit[31] for interrupt #159
  - Write 1 to clear bit to 0; write 0 has no effect
  - Read value indicates the current enable status |

Note: Controls might contain more than one register if there are more than 32 external interrupt inputs.
### Configuring the NVIC (2)

- **Set Pending & Clear Pending**
  - 0xE000E200-0xE000E21C, 0xE000E280-0xE000E29C

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E200</td>
<td>SETPEND0</td>
<td>R/W</td>
<td>0</td>
<td>Pending for external interrupt #0–31</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[0] for interrupt #0 (exception #16)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[1] for interrupt #1 (exception #17)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[31] for interrupt #31 (exception #47)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write 1 to set bit to 1; write 0 has no effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read value indicates the current status</td>
</tr>
<tr>
<td>0xE000E280</td>
<td>CLRPEND0</td>
<td>R/W</td>
<td>0</td>
<td>Clear pending for external interrupt #0–31</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[0] for interrupt #0 (exception #16)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[1] for interrupt #1 (exception #17)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[31] for interrupt #31 (exception #47)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write 1 to clear bit to 0; write 0 has no effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read value indicates the current pending status</td>
</tr>
</tbody>
</table>
Configuring the NVIC (3)

• Interrupt Active Status Register
  – 0xE000E300-0xE000E31C

Active Status

Each external interrupt has an active status bit. When the processor starts the interrupt handler, the bit is set to 1 and cleared when the interrupt return is executed. However, during an interrupt service routine execution, a higher-priority interrupt might occur and cause a preemption. During this period, despite the fact that the processor is executing another interrupt handler, the previous interrupt is still defined as active. The active registers are 32-bit but can also be accessed using half word or byte-size transfers. If there are more than 32 external interrupts, there will be more than one active register. The active status registers for external interrupts are read-only (see Table 8.4).

Table 8.4 Interrupt Active Status Registers (0xE000E300-0xE000E31C)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E300</td>
<td>ACTIVE0</td>
<td>R</td>
<td>0</td>
<td>Active status for external interrupt #0–31</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[0] for interrupt #0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[1] for interrupt #1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit[31] for interrupt #31</td>
</tr>
<tr>
<td>0xE000E304</td>
<td>ACTIVE1</td>
<td>R</td>
<td>0</td>
<td>Active status for external interrupt #32–63</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PRIMASK and FAULTMASK Special Registers

The PRIMASK register is used to disable all exceptions except NMI and hard fault. It effectively changes the current priority level to 0 (highest programmable level). This register is programmable using MRS and MSR instructions. For example:

```
MOV    R0, #1
MSR    PRIMASK, R0   ; Write 1 to PRIMASK to disable all
                      ; interrupts
```
Interrupt Priority

- What do we do if several interrupts arrive at the same time?
- NVIC allows to set priorities for (almost) every interrupt
- 3 fixed highest priorities, up to 256 programmable priorities
  - 128 preemption levels
  - Not all priorities have to be implemented by a vendor!

- Higher priority interrupts can pre-empt lower priorities
- Priority can be sub-divided into priority groups
  - splits priority register into two halves, preempt priority and subpriority
  - preempt priority: indicates if an interrupt can pre-empt another
  - subpriority: used if two interrupts of same group arrive concurrently
- Interrupt Priority Level Registers
  - 0xE000E400-0xE000E4EF

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E400</td>
<td>PRI_0</td>
<td>R/W</td>
<td>0 (8-bit)</td>
<td>Priority-level external interrupt #0</td>
</tr>
<tr>
<td>0xE000E401</td>
<td>PRI_1</td>
<td>R/W</td>
<td>0 (8-bit)</td>
<td>Priority-level external interrupt #1</td>
</tr>
<tr>
<td>...</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0xE000E41F</td>
<td>PRI_31</td>
<td>R/W</td>
<td>0 (8-bit)</td>
<td>Priority-level external interrupt #31</td>
</tr>
<tr>
<td>...</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Preemption Priority and Subpriority

When deciding the effective preempt priority level and subpriority level, you must take these factors into account:

- Implemented priority-level configuration registers
- Priority group setting

For example, if the width of the configuration registers is 3 (bit 7 to bit 5 are available) and priority group is set to 5, you can have four levels of preempt priority levels (bit 7 to bit 6), and inside each preempt level there are two levels of subpriority (bit 5).

<table>
<thead>
<tr>
<th>Priority Group</th>
<th>Preempt Priority Field</th>
<th>Subpriority Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Bit [7:1]</td>
<td>Bit [0]</td>
</tr>
<tr>
<td>1</td>
<td>Bit [7:2]</td>
<td>Bit [1:0]</td>
</tr>
<tr>
<td>2</td>
<td>Bit [7:3]</td>
<td>Bit [2:0]</td>
</tr>
<tr>
<td>3</td>
<td>Bit [7:4]</td>
<td>Bit [3:0]</td>
</tr>
<tr>
<td>4</td>
<td>Bit [7:5]</td>
<td>Bit [4:0]</td>
</tr>
<tr>
<td>5</td>
<td>Bit [7:6]</td>
<td>Bit [5:0]</td>
</tr>
<tr>
<td>6</td>
<td>Bit [7]</td>
<td>Bit [6:0]</td>
</tr>
<tr>
<td>7</td>
<td>None</td>
<td>Bit [7:0]</td>
</tr>
</tbody>
</table>

Table 7.4 Definition of Preempt Priority Field and Subpriority Field in a Priority Level Register in Different Priority Group Settings

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>VECTKEY</td>
<td>R/W</td>
<td>–</td>
<td>Access key; 0x05FA must be written to this field to write to this register, otherwise the write will be ignored; the read-back value of the upper half word is 0xFA05</td>
</tr>
<tr>
<td>15</td>
<td>ENDIANNESS</td>
<td>R</td>
<td>–</td>
<td>Indicates endianness for data: 1 for big endian (BE8) and 0 for little endian; this can only change after a reset</td>
</tr>
<tr>
<td>10:8</td>
<td>PRIGROUP</td>
<td>R/W</td>
<td>0</td>
<td>Priority group</td>
</tr>
<tr>
<td>2</td>
<td>SYSRESETREQ</td>
<td>W</td>
<td>–</td>
<td>Requests chip control logic to generate a reset</td>
</tr>
<tr>
<td>1</td>
<td>VECTCLRACTIVE</td>
<td>W</td>
<td>–</td>
<td>Clears all active state information for exceptions; typically used in debug or OS to allow system to recover from system error (Reset is safer)</td>
</tr>
<tr>
<td>0</td>
<td>VECTRESET</td>
<td>W</td>
<td>–</td>
<td>Resets the Cortex-M3 processor (except debug logic), but this will not reset circuits outside the processor</td>
</tr>
</tbody>
</table>
Exercise: How many preemption priorities and subpriority levels do we get on the Smart Fusion if we set Priority Group to 5?
What if we quickly want to disable all interrupts?

- Write 1 into PRIMASK to disable all interrupt except NMI
  - MOV R0, #1
  - MSR PRIMASK, R0
- Write 0 into PRIMASK to enable all interrupts
- FAULTMASK is the same as PRIMASK, but also blocks hard fault (priority -1)

What if we want to disable all interrupts below a certain priority?

- Write priority into BASEPRI
  - MOV R0, #0x60
  - MSR BASEPRI, R0
What exactly is an interrupt handler?
• Upon an interrupt, the Cortex-M3 needs to know the address of the interrupt handler (function pointer)
• After powerup, vector table is located at 0x00000000

<table>
<thead>
<tr>
<th>Address</th>
<th>Exception Number</th>
<th>Value (Word Size)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>–</td>
<td>MSP initial value</td>
</tr>
<tr>
<td>0x00000004</td>
<td>1</td>
<td>Reset vector (program counter initial value)</td>
</tr>
<tr>
<td>0x00000008</td>
<td>2</td>
<td>NMI handler starting address</td>
</tr>
<tr>
<td>0x0000000C</td>
<td>3</td>
<td>Hard fault handler starting address</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>Other handler starting address</td>
</tr>
</tbody>
</table>

• Can be relocated to change interrupt handlers at runtime (vector table offset register)
Vector Table in SoftConsole

- Located in startup_a2fxxxxm3.s

```asm
23 .globl g_pfnVectors
24 .word __estack
25 .word Reset_Handler
26 .word NMI_Handler
27 .word HardFault_Handler
28 .word MemManage_Handler
29 .word BusFault_Handler
30 .word UsageFault_Handler
31 .word 0
32 .word 0
```

- Put at 0x00000000 in linker script

```asm
42 SECTIONS
43 {
44 .text :
45 {
46 CREATE_OBJECT_SYMBOLS
47 __text_load = LOADADDR(.text);
48 __text_start = .;
49 *(.isr_vector)
```

39
Interrupt Handlers

192/****************************
193  * Reset_Handler
194  */
195  .global Reset_Handler
196  .type  Reset_Handler, %function
197 Reset_Handler:
198  _start:

280/****************************
281  * NMI_Handler
282  */
283  .weak NMI_Handler
284  .type  NMI_Handler, %function
285 NMI_Handler:
286  B .
287
288/****************************
289  * HardFault_Handler
290  */
291  .weak HardFault_Handler
292  .type  HardFault_Handler, %function
293 HardFault_Handler:
294  B .
295
• We can overwrite the predefined interrupt handlers

```c
__attribute__((__interrupt__)) void Timer1_IRQHandler()
{
    MSS_TIM1_disable_irq();
    MSS_TIM1_clear_irq();
    ...
    NVIC_ClearPendingIRQ( Timer1_IRQn );
}

int main()
{
    MSS_TIM1_enable_irq();
    NVIC_EnableIRQ( Timer1_IRQn );
    ...
    while(1) {} 
}
```
1. Automatic saving of registers upon exception
   • PC, PSR, R0-R3, R12, LR pushed on the stack
2. While bus busy, fetch exception vector
3. Update SP to new location
4. Update IPSR (low part of PSR) with new exception number
5. Set PC to vector handler
6. Update LR to special value EXC_RETURN

• Several other NVIC registers get updated
• Latency: as short as 12 cycles
Interrupt Stacking

The values of PC and PSR are stacked first so that instruction fetch can be started early (which requires modification of PC) and the IPSR can be updated early. After stacking, SP will be updated to \( N - 32 \) (0x1100320), and the stacked data arrangement in the stack memory will look like Table 9.1.

<table>
<thead>
<tr>
<th>Address (HADDR)</th>
<th>N-8</th>
<th>N-4</th>
<th>N-32</th>
<th>N-28</th>
<th>N-24</th>
<th>N-20</th>
<th>N-16</th>
<th>N-12</th>
</tr>
</thead>
</table>

The reason the registers R0–R3, R12, LR, PC, and PSR are stacked is that these are caller saved registers, according to C standards (C/C standard Procedure Call Standard for the ARM Architecture, AAPCS, Ref 5). This arrangement allows the interrupt handler to be a normal C function, because registers that could be changed by the exception handler are saved in the stack. The general registers (R0–R3, R12) are located at the end of the stack frame so that they can be easily accessed using SP-related addressing. As a result, it's easy to pass parameters to software interrupts using stacked registers.

**Figure 9.1 Stacking Sequence**

<table>
<thead>
<tr>
<th>Address (HADDR)</th>
<th>Old SP (N) - (Previously pushed data)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-8</td>
<td>(N-4) PSR 2</td>
</tr>
<tr>
<td>N-4</td>
<td>(N-8) PC 1</td>
</tr>
<tr>
<td>N-32</td>
<td>(N-12) LR 8</td>
</tr>
<tr>
<td>N-28</td>
<td>(N-16) R12 7</td>
</tr>
<tr>
<td>N-24</td>
<td>(N-20) R3 6</td>
</tr>
<tr>
<td>N-20</td>
<td>(N-24) R2 5</td>
</tr>
<tr>
<td>N-16</td>
<td>(N-28) R1 4</td>
</tr>
<tr>
<td>N-12</td>
<td>(N-32) R0 3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>New SP (N-32)</th>
<th></th>
</tr>
</thead>
</table>

**Table 9.1 Stack Memory Content After Stacking and Stacking Order**

- The data bus is busy stacking the registers.
- The instruction bus carries out another important task of the interrupt sequence: It fetches the exception vector (the starting address of the exception handler) from the vector table. Since the stacking and vector fetch are performed on separate bus interfaces, they can be carried out at the same time.

**Vector Fetches**

While the data bus is busy stacking the registers, the instruction bus carries out another important task of the interrupt sequence: It fetches the exception vector (the starting address of the exception handler) from the vector table. Since the stacking and vector fetch are performed on separate bus interfaces, they can be carried out at the same time.

You can read the program status registers using the MRS instruction. You can also change the APSR using the MSR instruction, but EPSR and IPSR are read-only. For example:

```
MRS r0, APSR     ; Read Flag state into R0
MRS r0, IPSR     ; Read Exception/Interrupt state
MRS r0, EPSR     ; Read Execution state
MSR APSR, r0     ; Write Flag state
```

In ARM assembler, when accessing xPSR (all three program status registers as one), the symbol `PSR` is used:

```
MRS r0, PSR     ; Read the combined program status word
MSR PSR, r0     ; Write combined program state word
```

The descriptions for the bit fields in PSR are shown in Table 3.1.

<table>
<thead>
<tr>
<th>Bit Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>N Negative</td>
<td>N</td>
</tr>
<tr>
<td>Z Zero</td>
<td>Z</td>
</tr>
<tr>
<td>C Carry/borrow</td>
<td>C</td>
</tr>
<tr>
<td>V Overflow</td>
<td>V</td>
</tr>
<tr>
<td>Q Sticky saturation flag</td>
<td>Q</td>
</tr>
<tr>
<td>ICI/IT Interrupt-Continuable Instruction (ICI) bits, IF-THEN instruction status bit</td>
<td>ICI/IT</td>
</tr>
<tr>
<td>T Thumb state, always 1; trying to clear this bit will cause a fault exception</td>
<td>T</td>
</tr>
<tr>
<td>Exception Indicates which exception the processor is handling</td>
<td>Number</td>
</tr>
</tbody>
</table>

**Figure 3.3 Program Status Registers (PSRs) in the Cortex-M3**

- From: The Definitive Guide to the ARM Cortex-M3

**Figure 3.4 Combined Program Status Registers (xPSR) in the Cortex-M3**

```
MRS r0, xPSR     ; Read the combined program status word
MSR xPSR, r0     ; Write combined program state word
```

<table>
<thead>
<tr>
<th>Bit Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>N Negative</td>
<td>N</td>
</tr>
<tr>
<td>Z Zero</td>
<td>Z</td>
</tr>
<tr>
<td>C Carry/borrow</td>
<td>C</td>
</tr>
<tr>
<td>V Overflow</td>
<td>V</td>
</tr>
<tr>
<td>Q Sticky saturation flag</td>
<td>Q</td>
</tr>
<tr>
<td>ICI/IT Interrupt-Continuable Instruction (ICI) bits, IF-THEN instruction status bit</td>
<td>ICI/IT</td>
</tr>
<tr>
<td>T Thumb state, always 1; trying to clear this bit will cause a fault exception</td>
<td>T</td>
</tr>
<tr>
<td>Exception Indicates which exception the processor is handling</td>
<td>Number</td>
</tr>
</tbody>
</table>

- From: The Definitive Guide to the ARM Cortex-M3
Return from ISR

• 3 ways to return from an ISR

<table>
<thead>
<tr>
<th>Return Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BX &lt;reg&gt;</td>
<td>If the EXC_RETURN value is still in LR, we can use the BX LR instruction to perform the interrupt return.</td>
</tr>
<tr>
<td>POP {PC}, or POP {..., PC}</td>
<td>Very often the value of LR is pushed to the stack after entering the exception handler. We can use the POP instruction, either a single POP or multiple POPs, to put the EXC_RETURN value to the program counter. This will cause the processor to perform the interrupt return.</td>
</tr>
<tr>
<td>LDR, or LDM</td>
<td>It is possible to produce an interrupt return using the LDR instruction with PC as the destination register.</td>
</tr>
</tbody>
</table>

• Unstack and reset SP
• Update NVIC registers
Nested Interrupts

• Built into the Cortex-M3 (not every MCU has this)
• Make sure main stack is large enough!

• Two methods:
  – Tail Chaining
  – Late Arrival (preemption)
Tail Chaining

- If first interrupt has same or higher priority
- Skip stacking/unstacking for efficiency
Late Arrival (Preemption)

• Main stack must be able to hold maximum number of preemptions!
Different Concepts of Interrupt Sharing

- Number of potential interrupts usually larger than interrupt lines availability on Core
- One peripheral often only has one interrupt
- Different types of events are stored in a status register

Example, UART – IIR, 0x40000008

<table>
<thead>
<tr>
<th>3:0</th>
<th>Interrupt identification bits</th>
<th>R</th>
<th>0b0001</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>Highest priority. Receiver line status interrupt due to overrun error, parity error, framing error or break interrupt. Reading the Line Status Register resets this interrupt.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Second priority. Receive data available interrupt modem status interrupt. Reading the Receiver Buffer Register (RBR) or the FIFO drops below the trigger level resets this interrupt.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b1100</td>
<td>Second priority. Character timeout indication interrupt occurs when no characters have been read from the RX FIFO during the last four character times and there was at least one character in it during this time. Reading the Receive Buffer Register (RBR) resets this interrupt.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b0010</td>
<td>Third priority. Transmitter Holding Register Empty interrupt. Reading the IIR or writing to the Transmitter Holding Register (THR) resets the interrupt.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b0000</td>
<td>Fourth priority. Modem status interrupt due to Clear to Send, Data Set Ready, Ring Indicator, or Data Carrier Detect being asserted. Reading the Modem Status Register resets this interrupt.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This register is read only; writing has no effect. Also see Table 15-9.
ISR Sharing, i.e., Callbacks in C

- There is only one interrupt handler
- Functions have to “subscribe” for events
- Callbacks
  - Driver provides function to register a function pointer
  - Driver stores function pointers in list
  - Upon interrupt, each registered function gets called

```c
typedef void (*radioalarm_handler_t)(void);
radioalarm_handler_t radio_alarm_fired;

void RadioAlarm_init(radioalarm_handler_t handler)
{
    radio_alarm_fired = handler;
}

__attribute__((__interrupt__)) void Timer1_IRQHandler()
{
    alarm_state = FREE;
    MSS_TIM1_disable_irq();
    MSS_TIM1_clear_irq();
    NVIC_ClearPendingIRQ(Timer1_IRQn);
    (*(radio_alarm_fired))(); // call the callback function
}
Common Problems and Pit-Falls

• Too many interrupts
  – Your core can’t keep up with handling interrupts

• Concurrency issues
  – One interrupt handler modifies global variables
  – Can be avoided using atomic sections protected through PRIMASK

• Lost interrupts
  – It can happen that an interrupt doesn’t get treated by the Core
  – State machine and peripheral has to be aware of this possibility
  – Danger for deadlocks
Summary

• Overwrite default Interrupt Handler

• Initialization
  – Enable interrupt in NVIC
  – Enable interrupt in Peripheral

• Upon Interrupt
  – Clear interrupt in Peripheral
  – Clear pending bit in NVIC
  – *Potentially disable interrupts temporarily*