Announcements

• Extra Lab Hours
  • http://goo.gl/kj8oL

• HW1.2 Notes
  • Do not put text or labels on Top Metal Layer. That’s what the silkscreen (Top Overlay) is for!

• Avoid direct pad connects on chips

• Do not ignore DFM errors
  • Vias too small
  • Insufficient text width
  • Signal Distance problems
  • Double drill hits
  • Insufficient spacing
Vias in Pad
Lab 1, Common Mistakes

• Verilog Language Issue
  – output [3:0] Y;
    Y = 4'b110
  – Correct, but looks strange

• Propagation delay usually measured from 50% point
Lab Reports

• Lab reports are due at the beginning of your next lab
  – If there are demos, than you have to do them within the first couple of minutes of the next lab session!

• Try to use Agilent IntuiLink (if it works)
  – Significantly better than snapshots or pictures
  – BUT: doesn’t work on all stations...

• Hand-in requirements
  – printed out or electronically to the TAs (not the ece5780.6780@gmail.com email for now!)
Minute Quiz
Advanced Microcontroller Bus Architecture (AMBA)
- Advanced High-performance Bus (AHB)
- Advanced Peripheral Bus (APB)
Internal and external busses are accessed in very different ways!

- Atmel SAM3U
  - Accessed physically w/ wires
  - Accessed logically w/ VHDL & Verilog
Why not just export the AHB-Lite or APB off-chip?
Outline

• Minute quiz

• Announcements

• Asynchronous Memory

• External Memory Controller

• Open Discussions
An SRAM chip and its asynchronous parallel interface

- **A**: 20-bit address bus
- **DQ**: 8-bit data bus
- **CE#**: chip enable
- **WE#**: write enable
- **OE#**: output enable

![Diagram of SRAM chip](image)

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>DQ1 to DQ8</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Not Selected</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Write</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>High Z</td>
</tr>
</tbody>
</table>
GS78108 read cycle...has no clock

![Diagram of GS78108 read cycle parameters]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read cycle time</td>
<td>$t_{RC}$</td>
</tr>
<tr>
<td>Address access time</td>
<td>$t_{AA}$</td>
</tr>
<tr>
<td>Chip enable access time (CE)</td>
<td>$t_{AC}$</td>
</tr>
<tr>
<td>Output enable to output valid (OE)</td>
<td>$t_{OE}$</td>
</tr>
<tr>
<td>Output hold from address change</td>
<td>$t_{OH}$</td>
</tr>
<tr>
<td>Chip enable to output in low Z (CE)</td>
<td>$t_{LZ}$</td>
</tr>
<tr>
<td>Output enable to output in low Z (OE)</td>
<td>$t_{OLZ}$</td>
</tr>
<tr>
<td>Chip disable to output in High Z (CE)</td>
<td>$t_{HZ}$</td>
</tr>
<tr>
<td>Output disable to output in High Z (OE)</td>
<td>$t_{OHZ}$</td>
</tr>
</tbody>
</table>
GS78108 WE#-controlled write cycle

Parameter | Symbol
---|---
Write cycle time | tWC
Address valid to end of write | tAW
Chip enable to end of write | tCW
Data set up time | tDW
Data hold time | tDH
Write pulse width | tWP
Address set up time | tAS
Write recovery time (WE) | tWR
Write recovery time (CE) | tWR1
Output Low Z from end of write | tWLZ
Write to output in High Z | tWHZ
GS78108 CE#-controlled write cycle

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write cycle time</td>
<td>tWC</td>
</tr>
<tr>
<td>Address valid to end of write</td>
<td>tAW</td>
</tr>
<tr>
<td>Chip enable to end of write</td>
<td>tCW</td>
</tr>
<tr>
<td>Data set up time</td>
<td>tDW</td>
</tr>
<tr>
<td>Data hold time</td>
<td>tDH</td>
</tr>
<tr>
<td>Write pulse width</td>
<td>tWP</td>
</tr>
<tr>
<td>Address set up time</td>
<td>tAS</td>
</tr>
<tr>
<td>Write recovery time (WE)</td>
<td>tWR</td>
</tr>
<tr>
<td>Write recovery time (CE)</td>
<td>tWR1</td>
</tr>
<tr>
<td>Output Low Z from end of write</td>
<td>tWLZ'</td>
</tr>
<tr>
<td>Write to output in High Z</td>
<td>tWHZ'</td>
</tr>
</tbody>
</table>
An asynchronous NOR flash memory
(that does not have a clock input line)

- A: 25-bit address bus
- DQ: A 16-bit data bus
- CE#: chip enable
- WE#: write enable
- OE#: output enable
- BYTE: 8-bit or 16-bit mode
- WP#/ACC: write protect
- RY/BY#: ready/busy
- RESET#: clear internal status
S29GL512P read cycle

Waveform | Inputs | Outputs
---|---|---
Steady |  |  
Changing from H to L |  |  
Changing from L to H |  |  
Don't Care, Any Change Permitted | Changing, State Unknown |  
Does Not Apply | Center Line is High Impedance State (High Z) |  

Addresses
CE#
OE#
WE#
Outputs
RESET#
RY/BY#
0 V
## S29GL512P Read Cycle Timing

### Table 11.3 S29GL-P Read-Only Operations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description (Notes)</th>
<th>Test Setup</th>
<th>Speed Options</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>JEDEC Std.</td>
<td></td>
<td></td>
<td>90 100 110 120 130</td>
<td></td>
</tr>
<tr>
<td>t\text{AVAV} t\text{RC}</td>
<td>Read Cycle Time</td>
<td>$V_{IO} = V_{CC} = 2.7 \text{ V}$</td>
<td>Min</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} \leq 1.65 \text{ V}$</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>-</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} = V_{CC} = 3.0 \text{ V}$</td>
<td>-</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t\text{AVQV} t\text{ACC}</td>
<td>Address to Output Delay (1)</td>
<td>$V_{IO} = V_{CC} = 2.7 \text{ V}$</td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} \leq 1.65 \text{ V}$</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>-</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} = V_{CC} = 3.0 \text{ V}$</td>
<td>-</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t\text{ELQV} t\text{CE}</td>
<td>Chip Enable to Output Delay (2)</td>
<td>$V_{IO} = V_{CC} = 2.7 \text{ V}$</td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} \leq 1.65 \text{ V}$</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>-</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} = V_{CC} = 3.0 \text{ V}$</td>
<td>-</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t\text{PACC}</td>
<td>Page Access Time</td>
<td></td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{GLOV} t\text{OE}</td>
<td>Output Enable to Output Delay</td>
<td></td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Max</td>
<td>25</td>
</tr>
<tr>
<td>t\text{EHQZ} t\text{DF}</td>
<td>Chip Enable to Output High Z (3)</td>
<td></td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Max</td>
<td>20</td>
</tr>
<tr>
<td>t\text{GHOZ} t\text{DF}</td>
<td>Output Enable to Output High Z (3)</td>
<td></td>
<td>Max</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Max</td>
<td>20</td>
</tr>
<tr>
<td>t\text{AXQX} t\text{OH}</td>
<td>Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First</td>
<td>Min</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>t\text{OEH}</td>
<td>Output Enable Hold Time (3)</td>
<td>Read</td>
<td>Min</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Toggle and Data# Polling</td>
<td>Min</td>
<td>10</td>
</tr>
<tr>
<td>t\text{CEH}</td>
<td>Chip Enable Hold Time</td>
<td></td>
<td>Min</td>
<td>35</td>
</tr>
</tbody>
</table>

1. $CE\#$, $OE\# = V_{IL}$
2. $OE\# = V_{IL}$
3. Not 100% tested.
4. See Figure 11.3 and Table 11.1 for test specifications.
5. Unless otherwise indicated, AC specifications for 110 ns speed options are tested with $V_{IO} = V_{CC} = 2.7 \text{ V}$. AC specifications for 110 ns speed options are tested with $V_{IO} = 1.8 \text{ V}$ and $V_{CC} = 3.0 \text{ V}$. 
LCD controller (PMO13701) exports both a parallel and a serial interface.

- 8-bit parallel interface
  - D: 8-bit data bus
  - BS1/BS2: Ifc mode select
  - CS#: chip select
  - RD#: read data
  - WR#: write data
  - RES#: hardware reset
  - D/C#: Slave address bit
• Minute quiz
• Announcements
• Asynchronous Memory
• External Memory Controller
• Open Discussions
Accessing external parallel devices

- AHB and APB are wide, de-multiplexed internal busses
- External busses tradeoff pin-count, performance, ...
  - ISA
  - VESA
  - AGP
  - PCI
  - VME
  - IDE
  - CF
- MCUs often integrate external memory controllers
  - Often tailored to specific peripheral class
  - EMCs ease memory/peripheral interfacing
• Provide glueless interface to external devices

• Asynchronous and Synchronous memories supported

• EMC is mapped into system address space
  - 0x70000000 to 0x77FFFFFF

• Offers
  - 2 chip select lines (CS)
  - 8-bit or 16-bit shared data bus
  - Write enable generation
  - Translates 32-bit AHB transfers into half-word and byte txns
  - Automatic translation of misaligned addresses
SmartFusion’s External Memory Controller

AHB Bus Matrix
EMC Slave Interface

External Memory Controller Block (EMC)

EMC_CS[1:0]_N
EMC_RW_N
EMC_BYTE_EN[1:0]
EMC_OEN[1:0]_N
EMC_PAD_OE
EMCWDB[15:0]
EMCRDB[15:0]

External Memory Device (EMD)
(Sync SRAM, Async SRAM, NOR FLASH)

SmartFusion
North and West I/Os

Microcontroller SubSystem

SysReg

EMC_CS_0_CR
EMC_CS_1_CR

EMC_MEMTYPE[0:1]
EMC_PORTSIZE0
EMC_RDLATFIRST[3:0]
EMC_RDLATREST[3:0]
EMC_WRLAT[0:3]
EMC_WRTAT[1:0]
EMC_PIPERDN0
EMC_PIPERW0
EMC_RWPOLO
EMC_WENBEN0
EMC_CSFE0

EMC_MEMTYPE[1:0]
EMC_PORTSIZE1
EMC_RDLATFIRST[3:0]
EMC_RDLATREST[3:0]
EMC_WRLAT1[3:0]
EMC_WRTAT1[1:0]
EMC_PIPERDN1
EMC_PIPERW1
EMC_RWPOLO1
EMC_WENBEN1
EMC_CSFE1

FCLK
FRESEn

HSEL
HADDR[24:0]
HSIZE[1:0]
HTRANS[1]
HWDATA[31:0]
HWRITE
HREADY
HRDATA[31:0]
HREADYOUT
HRESP

EMC_CLK
EMC_AB[25:0]

23
AHB read/write transfers

Diagram showing the timing of FCLK, HADDR[31:0], HWRITE, HRDATA[31:0], and HREADY signals during address and data phases.
EMC operation

- EMC accepts single AHB transactions
  - Reading external memory devices (EMD)
  - Writing EMD

- EMC reformats single AHB transactions into EMD format

- EMC may use multiple CLK cycles to complete access
  - Recall AHB transfers complete in two cycles

- EMC cannot complete EMD R/W in only two cycles

- User must configure EMC to include wait states
AHB read transfer with two wait states
EMC operation continued

- EMC uses extra cycles to complete EMD transaction
- AHB address phase is one cycle (wait states are in data)
- EMC requires one cycle to output EMD address
- EMD requires two cycles to fetch the data
- EMC requires one additional cycle to transfer data to AHB
- A total of three wait states on AHB transfers
Byte-Wide External Memory Device

**AHB Address HADDR [31:0]**

- **Upper 64M of AHB Memory Space**
  - 0x77FFFFFF – 0x77FFFFFC
  - 0x77FFFFFFB – 0x77FFFFFB

- **Lower 64M of AHB Memory Space**
  - 0x74000003 – 0x74000000
  - 0x77FFFFFF – 0x73FFFFFC

**AHB Data H(R/W)DATA[31:0]**

**EMC_DB[7:0]**

- 0x00000000
- 0x03FFFFFF
- 0x00000001
- 0x03FFFFFC
- 0x03FFFFFE
- 0x03FFFFFD
- 0x03FFFFFF
- 0x03FFFFFE

**EMC_AB[25:0]**

- 0x00000000
- 0x03FFFFFF
- 0x03FFFFFC
- 0x03FFFFFE
- 0x03FFFFFD
- 0x03FFFFFF
- 0x03FFFFFE
- 0x00000001

**EMC_CS1_N**

- 0x00000000
- 0x03FFFFFC
- 0x03FFFFFE
- 0x03FFFFFD
- 0x03FFFFFF
- 0x03FFFFFE
- 0x00000001

**EMC_CS0_N**

- 0x00000000
- 0x03FFFFFC
- 0x03FFFFFE
- 0x03FFFFFD
- 0x03FFFFFF
- 0x03FFFFFE
- 0x00000001
Half-Word Wide External 2x8-bit memory

### AHB Data H(R/W)DATA[31:0]

- **Upper 64M of AHB Memory Space**
  - HADDR [31:0]: 0x77FFFFFF – 0x77FFFFFFFC
  - HADDR [31:0]: 0x74000003 – 0x74000000

- **Lower 64M of AHB Memory Space**
  - HADDR [31:0]: 0x70000007 – 0x70000004
  - HADDR [31:0]: 0x70000003 – 0x70000000

### AHB Address HADDR[31:0]

- **64M External Memory Space**
  - HADDR [31:0]: 0x77FFFFFB – 0x77FFFFF8
  - HADDR [31:0]: 0x77FFFFFF – 0x77FFFFFC
  - HADDR [31:0]: 0x70000007 – 0x70000004

### Byte Wide External Memory Device Memory Map

- **Upper 64M of AHB Memory Space**
  - HADDR [31:0]: 0x77FFFFFF – 0x77FFFFFC
  - HADDR [31:0]: 0x70000007 – 0x70000004

- **Lower 64M of AHB Memory Space**
  - HADDR [31:0]: 0x77FFFFFF – 0x73FFFFFC
  - HADDR [31:0]: 0x70000003 – 0x70000000

### 64M External Memory Space

- **EMC_AB[25:0]**
  - EMC_AB[25:0]: 0x03FFFFFF – 0x03FFFFFD
  - EMC_AB[25:0]: 0x03FFFFFE – 0x03FFFFFC

- **EMC_DB[7:0]**
  - EMC_DB[7:0]: 0x03FFFFFF – 0x03FFFFFC
  - EMC_DB[7:0]: 0x03FFFFFD – 0x03FFFFFD

- **EMC_CS0_N**
  - EMC_CS0_N: 0x00000000
  - EMC_CS0_N: 0x00000001

- **EMC_CS1_N**
  - EMC_CS1_N: 0x00000000
  - EMC_CS1_N: 0x00000001
Using the EMC to attach four GS78108’s

- Four asynchronous SRAMs
- Byte enables used as write enables
Using the EMC to attach two S29GL512’s

- Two byte-mode NOR flash devices
- Byte enables used as write enables
AHB Data H(R/W)DATA[31:0]

<table>
<thead>
<tr>
<th>[31:24]</th>
<th>[23:16]</th>
<th>[15:8]</th>
<th>[7:0]</th>
</tr>
</thead>
</table>

Upper 64M of AHB Memory Space

<table>
<thead>
<tr>
<th>[31:24]</th>
<th>[23:16]</th>
<th>[15:8]</th>
<th>[7:0]</th>
</tr>
</thead>
</table>

Lower 64M of AHB Memory Space

<table>
<thead>
<tr>
<th>[31:24]</th>
<th>[23:16]</th>
<th>[15:8]</th>
<th>[7:0]</th>
</tr>
</thead>
</table>

AHB Address HADDR [31:0]

| [31:24] | [23:16] | [15:8] | [7:0] |

64M External Memory Space

<table>
<thead>
<tr>
<th>0x77FFFFFFF – 0x77FFFFFFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x77FFFFFFF – 0x77FFFFFFF</td>
</tr>
</tbody>
</table>

EMC_CS1_N

<table>
<thead>
<tr>
<th>0x74000003 – 0x74000000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x74000003 – 0x74000000</td>
</tr>
</tbody>
</table>

EMC_DB[15:0]

| [15:8] | [7:0] |

64M External Memory Space

<table>
<thead>
<tr>
<th>0x03FFFFFF – 0x03FFFFFE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x03FFFFFF – 0x03FFFFFE</td>
</tr>
</tbody>
</table>

EMC_AB[25:0]

| [15:8] | [7:0] |

64M External Memory Space

<table>
<thead>
<tr>
<th>0x00000001 – 0x00000000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000001 – 0x00000000</td>
</tr>
</tbody>
</table>

From: SmartFusion MSS User Guide
Using the EMC to interface with a synchronous SRAM

External Memory Device Examples

Figure 7-12 gives an overview of how to connect external memories to the EMC. While not exhaustive, the examples given are intended to provide the user with a sense of what the EMC is capable of.

Figure 7-12 shows a typical x16 SRAM connected to the EMC of a SmartFusion cSoC. An eight megabyte device is shown. The address bus is halfword aligned (A[17:0] = EMC_AB[18:1], since EMC_AB is a byte address). The halfword synchronous SRAM (16-bit) device uses the byte enable control pins to affect a single byte write.

The circuit of Figure 7-13 shows a representative configuration of synchronous SRAM for the SmartFusion EMC. Eight megabyte SSRAMS are shown. The address bus is again halfword aligned (A[21:0] = EMC_AB[22:1], since EMC_AB is a byte address).
Outline

• Minute quiz

• Announcements

• Asynchronous Memory

• External Memory Controller

• Open Discussions
Questions?

Comments?

Discussion?