Beagle Board

By Mark Thueson
Outline

- What you get
- Basic specs
- Use of board/projects
- Physical board (chips, ports)
- System overview
- Processor overview
- Development
What you get

- $50
- Board
- Micro SD
- SD Adapter
- Box
- Foam
- No cables!
Basic specs/features

- Super-scalar ARM Cortex TM-A8 1GHz
- 512-MB LPDDR RAM
- High-speed USB 2.0 OTG port optionally powers the board
- On-board four-port high-speed USB 2.0 hub with 10/100 Ethernet
- DVI-D (digital computer monitors and HDTVs)
- S-video (TV out)
- Stereo audio out/in
- High-capacity microSD slot and 4-GB microSD card
- JTAG
- Camera port
New to xM

- Current measurement
- Overvoltage protection
- Serial port connection
- Audio expansion
- On board USB hub
- Camera port
- Expansion header
  - Pin muxing
Possible projects

• Web services
• 3-D gaming
• 3-D UI
• Linux kernel and driver development
• Boot loaders and firmware
• UI framework
• ARM® NEON codecs
• Codec plug-ins for GStreamers
• OpenGL® applications
• OpenMAX™ IL applications
• Ubuntu™, Android™, Windows embedded Debian etc.
• Home media centers
• In-vehicle entertainment
• Robotics
• Web kiosks
• And many more...!
My favorites

- Fire detection
- Home security system
- Copter
- Jukebox
- EInk
- Not inherently open source
Basic Ports

• USB OTG – power only
• 4 USB inputs
• Adapter Power
• JTAG
• Serial
• S-video
• DVI – no HDMI support
• Audio in/out
• Micro SD
Basic Ports
Expansions

- Expansion boards
  - Daughter card
- Camera
- LCD
- Audio
- Battery
Board Layout
System Diagram

DM3730 w/POP

DVI-D

Svideo

McBSP

Audio

LCD

Expansion

MMCEXP

Reset

User

USB HUB

JTAG

Host 1-4

Ethernet

microSD

RS232

Board Power

CLOCK

OVP

BeagleBoard-xM

Block Diagram
Processor Details

• Texas Instruments DM3730CBP “Da Vinci”
• 20 million polygons/sec graphics
• 188 General-Purpose I/O
• 12 32-bit General Purpose Timers
• Caches
  • 32KB L1 Program RAM
  • 80KB L1 Data RAM
  • 64KB L2 4-way associative
  • 32KB Shared L2 SRAM and 16KB L2 ROM
Micron 4Gb MDDR SDRAM (512MB) 200MHz
POP Advantages

- Memory device is separate from the logic device
  - The memory package can be tested separately from the logic package
  - If one is bad the other can still be used, unlike stacked-die packages
  - Memory from different suppliers can be used at different times without changing the logic.
- Any mechanically mating top package can be used.
- Minimized track length, faster signal propagation and less noise
Core Details

- Cortex A8
  - TrustZone
  - Thumb-2
- Neon – SIMD vector processing
  - Need special directive/instructions
- Level 1 Caches – both 16KByte, 4 way set associative
- Integrated 256 KB unified Level 2 Cache, 8-way set associative
- Two internal co-processors
  - Debug co-processor
  - System control co-processor
- Preload engine
  - Similar to DMA
  - Moves cache lines to/from L2
  - Two channels
Core pipeline

13-Stage Integer Pipeline

10-Stage NEON Pipeline
Development

- Debug – JTAG, few LEDs, one button, GPIO
- Community – Forums and Google repo
Questions?